

128LT SP0.5

Hybrid pyroelectric linear array with 128 responsive elements and integrated CMOS multiplexer

Description

The pyroelectric linear array 128LT SP0.5 is a hybrid detector with 128 responsive elements and an integrated CMOS multiplexer.

The pyroelectric chip consists of lithium tantalate (LiTaO_3). The size of the responsive elements is $90 \mu\text{m} \times 500 \mu\text{m}$ with a pitch of $100 \mu\text{m}$ ($90 \mu\text{m} \times 1000 \mu\text{m}$ available on request).

The multiplexer includes low-noise preamplifiers for each pixel, analogue switches and an output amplifier. The preamplifiers transform the signal charges of each pixel in a signal voltage, realize a band limiting and give the amplified signal to the sample&hold for the read-out process. The digital inputs are CMOS compatible.

For the measurement of the detector temperature a sensor (type AD 590) is integrated. It provides a temperature proportional current.

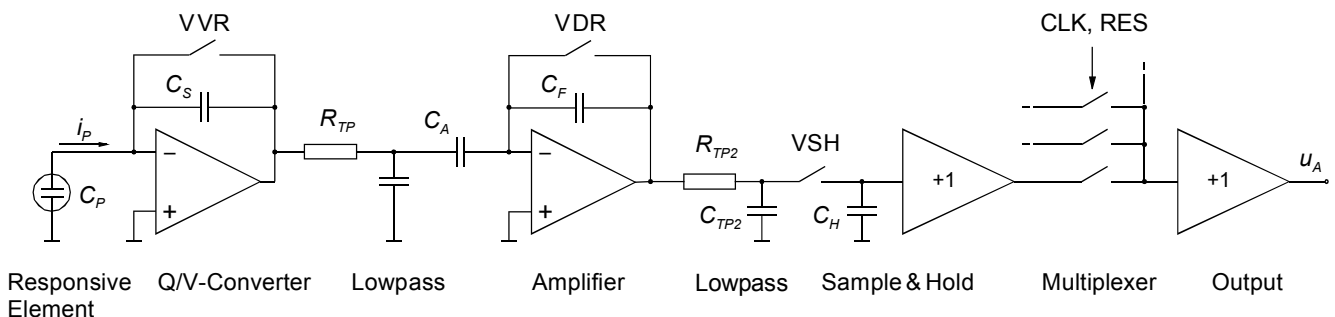
The pyroelectric chip and the read-out circuit are arranged in a metal hermetic package with an infrared window. It determines the spectral responsivity.

For the measurement of the infrared radiation it is necessary to chop the radiation flux.

Features

- 128 responsive elements arranged in a line
- Coated silicon as infrared window
- Broad band windows or special filters are possible on request
- NEP (128 Hz) = 4 nW (typical)
- Dynamic range > 75 dB
- Integrated CMOS multiplexer
- Good long-term stability
- Simple mode of operation
- Operation at ambient temperature
- Small package

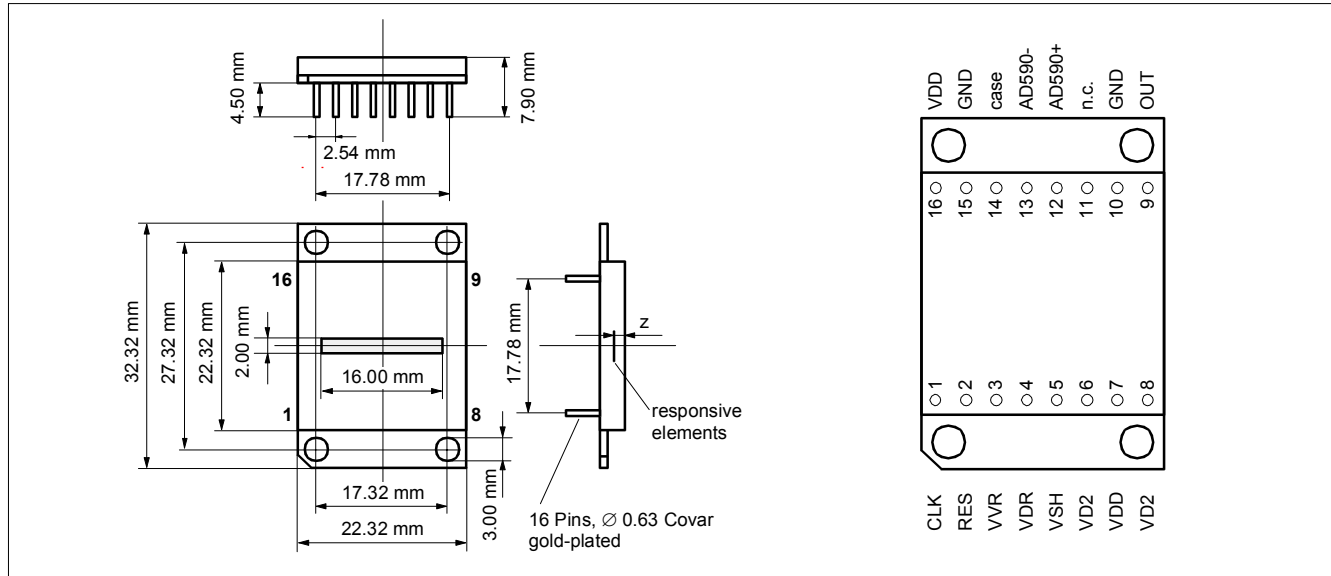
Readout-circuit



All parameters may change without notice due to new product development. 4/2006

Detector geometry and optical specification

Package and pins



Pins

Pin number	Pin name	Remark
1	CLK	Input clock CLK (trigger on rising edge)
2	RES	Input clock RES (active low)
3	VVR	Input clock VVR (active high)
4	VDR	Input clock VDR (active high)
5	VSH	Input clock VSH (active high)
6	VD2	Operating voltage (+2.5 V)
7	VDD	Operating voltage (+5 V)
8	VD2	Operating voltage (+2.5 V)
9	OUT	Analog signal output
10	GND	Ground
11	n. c.	not connected
12	AD590+	Temperature sensor
13	AD590-	Temperature sensor
14	case	case
15	GND	Ground
16	VDD	Operating voltage (+5 V)

Connect Pin 6 to Pin 8 (VD2), Pin 7 to Pin 16 (VDD), Pin 10 to Pin 15 (GND)

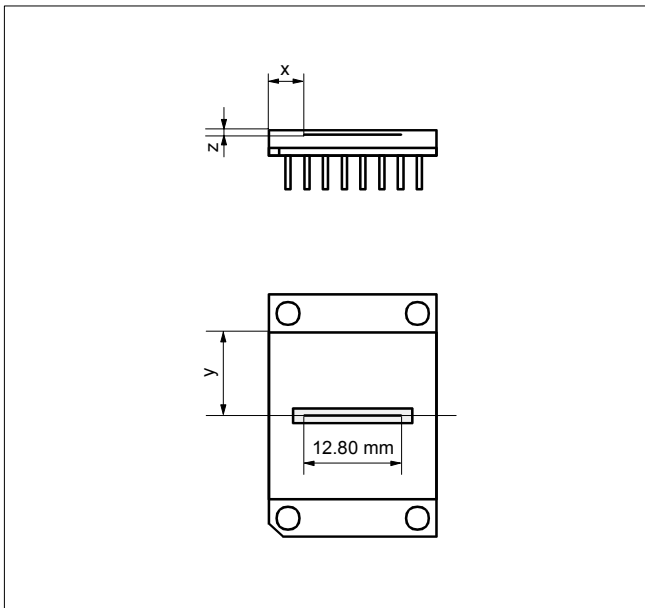
Optical Specification

Geometry

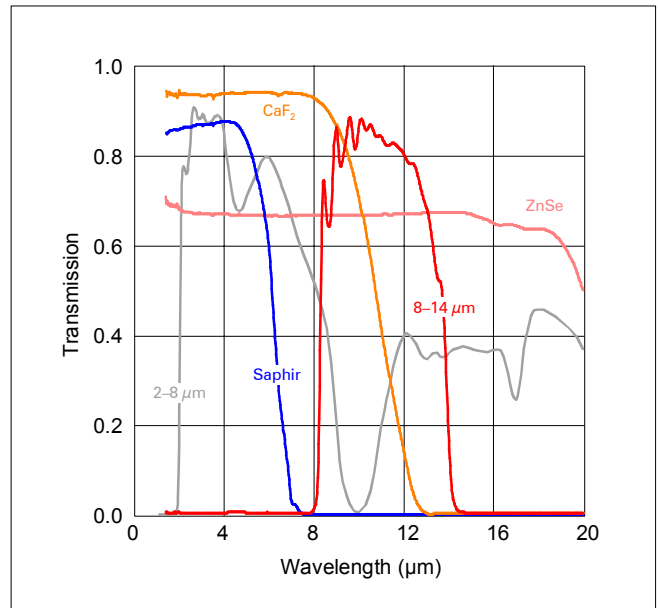
Parameter	Minimum value	Typical value	Maximum value	Unit
Field of view of each pixel ¹	90			°
Pixel width		90		µm
Pixel length		500		µm
Pitch		100		µm
Distance x	4.71	4.76	4.81	mm
Distance y	11.06	11.16	11.26	mm
Distance z	1.00	1.05	1.10	mm

¹ Perpendicular to the array

Position of the Pixels



Transmission of the window



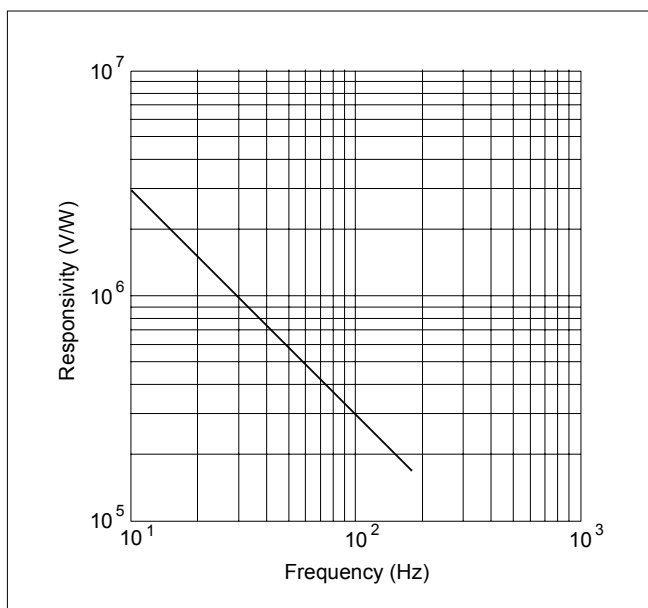
Electro-optical specification

Rectangular chopping with 128 Hz, array temperature 25 °C, black body source temperature 400 °C, filter transmission 100 %

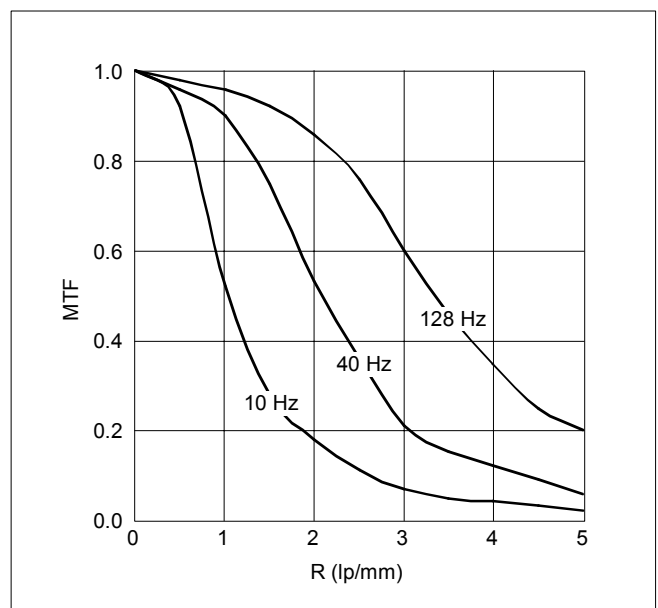
Parameter	Minimum value	Typical value	Maximum value	Unit
Responsivity S_V	196 000	230 000		V/W
Noise U_N		0.9	1.1	mV
NEP		3.9	5.6	nW
MTF ($R = 3$ lp/mm)	0.4	0.6		
Uniformity ¹ S_V		1	3	%
Operating temperature	-15		70	°C

¹ No defective elements

Typical responsivity



Typical MTF



Electrical parameters

All values for VDD = 5 V, VD2 = 2.5 V

Parameter	Minimum value	Typical value	Maximum value	Unit
VDD	4.75	5.0	5.25	V
VD2	2.4	2.5	2.6	V
Digital inputs				
Low voltage	0		0.3 VDD	V
High voltage	0.7 VDD		VDD	V
Switching threshold		0.5 VDD		V
Leakage current			±1	μA
Current consumption <i>I</i>		8		mA
AD590 Operating voltage ¹	4		30	V

¹ See data sheet of Analog Devices

Maximum/minimum conditions

All voltages refer to Ground (pin 10, 15)

Parameter	Maximum/minimum value	Unit
VDD, VD2	-0.3 to 7	V
Digital inputs CLK, RES, VVR, VDR, VSH	-0.3 to VDD 0.3	V
Chopping frequency f_{Ch}	10 to 512	Hz
AD590+ to AD590- ¹	-20 to 44	V
Analog output ²	±5	mA
Maximum irradiance	50	mW/mm ²
Soldering temperature (10 s)	300	°C
Storage temperature	-20 to 80	°C

¹ Potential free to ground (Pin 15), ² Not short resistant

Clock parameters

All values for VDD = 5 V, VD2 = 2.5 V

Parameter	Relative value	Minimum value	Typical value	Maximum value	Unit
Chopping frequency ¹ f_{Ch}		10	128	512	Hz
Readout clock CLK $f_{CLK} = 2 \cdot f_{Ch} \cdot 268$	$1 / t_{CLK}$	0	69	300	kHz
Reset clock low-impulse duration t_{RES}	$1/2 t_{CLK}$	1.8	7.5		μs
Clock VVR high-impulse duration t_{VVR}	$2 t_{CLK}$	7.5	30		μs
Clock VDR high-impulse duration t_{VDR}	$28 t_{CLK}^2$	200	400		μs
Clock VSH high-impulse duration t_{VSH}	$1 t_{CLK}$	3.5	15		μs
Settling time at the output t_{out}			1		μs

¹ $t_{Ch\ low} = t_{Ch\ high}$

² for $f_{Ch} = 512\ Hz$ t_{VDR} should be $56 \cdot t_{CLK} = 200\ \mu s$

Clock diagram

